ABSTRACT OF THE DISCLOSURE

Data Transfer Between an External Data Source and a Memory associated with a Data Processor

A data processor core 10 comprising a memory access interface portion 30 operable to perform data transfer operations between an external data source and at least one memory associated with said data processor core and a data processing portion 12 operable to perform further data processing operations in response to receipt of said processor clock signal CLK. The two portions of the core being operable to be independently enabled such that one portion may be active while the other is inactive.

Fig 1